4 Intel Fpga And Soc

This book constitutes the refereed proceedings of the 10th Annual Conference on Advanced Computer Architecture, ACA 2014, held in Shenyang, China, in August 2014. The 19 revised full papers presented were carefully reviewed and selected from 115 submissions. The papers are organized in topical sections on processors and circuits; high performance computing; GPUs and accelerators; cloud and data centers; energy and reliability; intelligence computing and mobile computing. Using the book and the software provided with it, the reader can build his/her own tester arrangement to investigate key aspects of analog-, digital- and mixed system circuits Plan of attack based on traditional testing, circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork, practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively This book constitutes the proceedings of the workshops of the 23rd International Conference on Parallel and Distributed Computing, Euro-Par 2017, held in Santiago de Compostela. Spain in August 2017. The 59 full papers presented were carefully reviewed and selected from 119 submissions. Euro-Par is an annual, international conference in Europe,

covering all aspects of parallel and distributed processing. These range from theory to practice, from small to the largest parallel and distributed systems and infrastructures, from fundamental computational problems to full-edged applications, from architecture, compiler, language and interface design and implementation to tools, support infrastructures, and application performance aspects.

This book provides wide knowledge about designing FPGA-based heterogeneous computing systems, using a high-level design environment based on OpenCL (Open Computing language), which is called OpenCL for FPGA. The OpenCL-based design methodology will be the key technology to exploit the potential of FPGAs in various applications such as low-power embedded applications and high-performance computing. By understanding the OpenCL-based design methodology, readers can design an entire FPGA-based computing system more easily compared to the conventional HDL-based design, because OpenCL for FPGA takes care of computation on a host, data transfer between a host and an FPGA, computation on an FPGA with a capable of accessing external DDR memories. In the step-by-step way, readers can understand followings: how to set up the design environment how to write better codes systematically considering architectural constraints how to design practical

applications

This book contains extended and revised versions of the best papers that were p- sented during the 16th edition of the IFIP/IEEE WG10.5 International Conference on Very Large Scale Integration, a global System-on-a-Chip Design & CAD conference. The 16th conference was held at the Grand Hotel of Rhodes Island, Greece (October 13–15, 2008). Previous conferences have taken place in Edinburgh, Trondheim, V- couver, Munich, Grenoble, Tokyo, Gramado, Lisbon, Montpellier, Darmstadt, Perth, Nice and Atlanta. VLSI-SoC 2008 was the 16th in a series of international conferences sponsored by IFIP TC 10 Working Group 10.5 and IEEE CEDA that explores the state of the art and the new developments in the field of VLSI systems and their designs. The purpose of the conference was to provide a forum to exchange ideas and to present industrial and research results in the fields of VLSI/ULSI systems, embedded systems and - croelectronic design and test.

Debugging Embedded and Real-Time Systems: The Art, Science, Technology and Tools of Real-Time System Debugging gives a unique introduction to debugging skills and strategies for embedded and real-time systems. Practically focused, it draws on application notes and white papers written by the companies who create design and debug tools. Debugging Embedded and Real Time Systems

presents best practice strategies for debugging real-time systems, through real-life case studies and coverage of specialized tools such as logic analysis, JTAG debuggers and performance analyzers. It follows the traditional design life cycle of an embedded system and points out where defects can be introduced and how to find them and prevent them in future designs. It also studies application performance monitoring, the execution trace recording of individual applications, and other tactics to debug and control individual running applications in the multitasking OS. Suitable for the professional engineer and student, this book is a compendium of best practices based on the literature as well as the author's considerable experience as a tools' developer. Provides a unique reference on Debugging Embedded and Real-Time Systems Presents best practice strategies for debugging real-time systems Written by an author with many years of experience as a tools developer Includes real-life case studies that show how debugging skills can be improved Covers logic analysis, JTAG debuggers and performance analyzers that are used for designing and debugging embedded systems

This book constitutes the proceedings of the 15th International Symposium on Applied Reconfigurable Computing, ARC 2019, held in Darmstadt, Germany, in April 2019. The 20 full papers and 7 short papers presented in this volume were carefully reviewed

and selected from 52 submissions. In addition, the volume contains 1 invited paper. The papers were organized in topical sections named: Applications; partial reconfiguration and security; image/video processing; high-level synthesis; CGRAs and vector processing; architectures; design frameworks and methodology; convolutional neural networks.

The fourth edition of Embedded Systems takes a big leap from the fundamentals of hardware to Edge Computing, Embedded IoT & Embedded AI. The book discusses next generation embedded systems topics, such as embedded SoC, Exascale computing systems and embedded systems' tensor processing units. This thoroughly updated edition serves as a textbook for engineering students and reference book for students of software-training institutions and embedded-systems-design professionals. Salient Features: 1. New chapters on IoT system architecture and design & Embedded AI 2. Case studies, such as, of Automatic Chocolate Vending Machine and Automobile Cruise Control 3. Bloom's Taxonomy-based chapter structure 4. Rich Pedagogy o 1000+ Self-assessment questions o 150+ MCQs o 220+ Review questions o 200+ Practice exercises

This book constitutes the refereed post-conference proceedings of 13 workshops held at the 34th International ISC High Performance 2019 Conference, in Frankfurt, Germany, in June 2019:

HPC I/O in the Data Center (HPC-IODC), Workshop on Performance & Scalability of Storage Systems (WOPSSS), Workshop on Performance & Scalability of Storage Systems (WOPSSS), 13th Workshop on Virtualization in High-Performance Cloud Computing (VHPC '18), 3rd International Workshop on In Situ Visualization: Introduction and Applications, ExaComm: Fourth International Workshop on Communication Architectures for HPC, Big Data, Deep Learning and Clouds at Extreme Scale, International Workshop on OpenPOWER for HPC (IWOPH18), IXPUG Workshop: Many-core Computing on Intel, Processors: Applications, Performance and Best-Practice Solutions, Workshop on Sustainable Ultrascale Computing Systems, Approximate and Transprecision Computing on Emerging Technologies (ATCET), First Workshop on the Convergence of Large Scale Simulation and Artificial Intelligence, 3rd Workshop for Open Source Supercomputing (OpenSuCo), First Workshop on Interactive High-Performance Computing, Workshop on Performance Portable Programming Models for Accelerators (P^3MA). The 48 full papers included in this volume were carefully reviewed and selected. They cover all aspects of research, development, and application of large-scale, high performance experimental and commercial systems. Topics include HPC computer architecture and hardware; programming models, system software, and

applications; solutions for heterogeneity, reliability, power efficiency of systems; virtualization and containerized environments; big data and cloud computing; and artificial intelligence.

Today, online technologies are at the core of most fields of engineering and society as a whole . This book discusses the fundamentals, applications and lessons learned in the field of online and remote engineering, virtual instrumentation, and other related technologies like Cross Reality, Data Science & Big Data, Internet of Things & Industrial Internet of Things, Industry 4.0, Cyber Security, and M2M & Smart Objects. Since the first Remote Engineering and Virtual Instrumentation (REV) conference in 2004, the event has focused on the use of the Internet for engineering tasks, as well as the related opportunities and challenges. In a globally connected world, interest in online collaboration, teleworking, remote services, and other digital working environments is rapidly increasing. In this context, the REV conferences discuss fundamentals, applications and experiences in the field of Online and Remote Engineering as well as Virtual Instrumentation. Furthermore, the conferences focus on guidelines and new concepts for engineering education in higher and vocational education institutions, including emerging technologies in learning, MOOCs & MOOLs, and open resources. This book presents the proceedings of REV2020 on

"Cross Reality and Data Science in Engineering" which was held as the 17th in series of annual events. It was organized in cooperation with the Engineering Education Transformations Institute and the Georgia Informatics Institutes for Research and Education and was held at the College of Engineering at the University of Georgia in Athens (GA), USA, from February 26 to 28, 2020.

The number of Android devices running on Intel processors has increased since Intel and Google announced, in late 2011, that they would be working together to optimize future versions of Android for Intel Atom processors. Today, Intel processors can be found in Android smartphones and tablets made by some of the top manufacturers of Android devices, such as Samsung, Lenovo, and Asus. The increase in Android devices featuring Intel processors has created a demand for Android applications optimized for Intel Architecture: Android Application Development for the Intel® Platform is the perfect introduction for software engineers and mobile app developers. Through well-designed app samples, code samples and case studies, the book teaches Android application development based on the Intel platform—including for smartphones, tablets, and embedded devices—covering performance tuning, debugging and optimization. This book is jointly developed for individual learning by Intel Software College and China Shanghai JiaoTong

University.

Embedded Systems - SoC, IoT, AI and Real-Time Systems | 4th EditionMcGraw-Hill Education

This book describes RTL design, synthesis, and timing closure strategies for SOC blocks. It covers high-level RTL design scenarios and challenges for SOC design. The book gives practical information on the issues in SOC and ASIC prototyping using modern high-density FPGAs. The book covers SOC performance improvement techniques, testing, and system-level verification. The book also describes the modern Xilinx FPGA architecture and their use in SOC prototyping. The book covers the Synopsys DC, PT commands, and use of them to constraint and to optimize SOC design. The contents of this book will be of use to students, professionals, and hobbyists alike.

The book includes the best extended papers which were selected from the 3rd International Conference of Electrical and Information Technologies (ICEIT 2017, Morocco). The book spans two inter-related research domains which shaped modern societies, solved many of their development problems, and contributed to their unprecedented economic growth and social welfare. Selected papers are based on original and high quality research. They were peer reviewed by experts in the field. They are grouped into five parts. Part I deals with Power System and Electronics topics that include Power Electronics &

Energy Conversion, Actuators & Micro/Nanotechnology, etc. Part II relates to Control Systems and their applications. Part III concerns the topic of Information Technology that basically includes Smart Grid, Information Security, Cloud Computing Distributed, Big Data, etc. Part IV discusses Telecommunications and Vehicular Technologies topics that include, Green Networking and Communications, Wireless Ad-hoc and Sensor Networks, etc. Part V covers Green Applications and Interdisciplinary topics, that include intelligent and Green Technologies for Transportation Systems, Smart Cities, etc. This book offers a good opportunity for young researchers, novice scholars and whole academic sphere to explore new trends in Electrical and information Technologies.

The book is divided into four major parts. Part I covers HDL constructs and synthesis of basic digital circuits. Part II provides an overview of embedded software development with the emphasis on low–level I/O access and drivers. Part III demonstrates the design and development of hardware and software for several complex I/O peripherals, including PS2 keyboard and mouse, a graphic video controller, an audio codec, and an SD (secure digital) card. Part IV provides three case studies of the integration of hardware accelerators, including a custom GCD (greatest common divisor) circuit, a Mandelbrot set fractal circuit, and an audio

synthesizer based on DDFS (direct digital frequency synthesis) methodology. The book utilizes FPGA devices, Nios II soft–core processor, and development platform from Altera Co., which is one of the two main FPGA manufactures. Altera has a generous university program that provides free software and discounted prototyping boards for educational institutions (details at http://www.altera.com/university). The two main educational prototyping boards are known as DE1 ($99) and DE2 ($269). All experiments can be implemented and tested with these boards. A board combined with this book becomes a “turn–key” solution for the SoPC design experiments and projects. Most HDL and C codes in the book are device independent and can be adapted by other prototyping boards as long as a board has similar I/O configuration.

Modeling, Operation, and Analysis of DC Grids presents a unified vision of direct current grids with their core analysis techniques, uniting power electronics, power systems, and multiple scales of applications. Part one presents high power applications such as HVDC transmission for wind energy, faults and protections in HVDC lines, stability analysis and inertia emulation. The second part addresses current applications in low voltage such as microgrids, power trains and aircraft applications. All chapters are self-contained with

numerical and experimental analysis. Provides a unified, coherent presentation of DC grid analysis based on modern research in power systems, power electronics, microgrids and MT-HVDC transmission Covers multiple scales of applications in one location, addressing DC grids in electric vehicles, microgrids, DC distribution, multi-terminal HVDC transmission and supergrids Supported by a unified set of MATLAB and Simulink test systems designed for application scenarios

A Multi-Processor System-on-Chip (MPSoC) is the key component for complex applications. These applications put huge pressure on memory, communication devices and computing units. This book, presented in two volumes – Architectures and Applications – therefore celebrates the 20th anniversary of MPSoC, an interdisciplinary forum that focuses on multi-core and multi-processor hardware and software systems. It is this interdisciplinarity which has led to MPSoC bringing together experts in these fields from around the world, over the last two decades. Multi-Processor System-on-Chip 1 covers the key components of MPSoC: processors, memory, interconnect and interfaces. It describes advance features of these components and technologies to build efficient MPSoC architectures. All the main components are detailed: use of memory and their technology, communication support and consistency, and

specific processor architectures for general purposes or for dedicated applications.

The 11 th IFIP International Conference on Very Large Scale Integration, in Montpellier, France, December 3-5,2001, was a great success. The main focus was about IP Cores, Circuits and System Designs & Applications as well as SOC Design Methods and CAD. This book contains the best papers (39 among 70) that have been presented during the conference. Those papers deal with all aspects of importance for the design of the current and future integrated systems. System on Chip (SOC) design is today a big challenge for designers, as a SOC may contain very different blocks, such as microcontrollers, DSPs, memories including embedded DRAM, analog, FPGA, RF front-ends for wireless communications and integrated sensors. The complete design of such chips, in very deep submicron technologies down to 0.13 mm, with several hundreds of millions of transistors, supplied at less than 1 Volt, is a very challenging task if design, verification, debug and industrial test are considered. The microelectronic revolution is fascinating; 55 years ago, in late 1947, the transistor was invented, and everybody knows that it was by William Shockley, John Bardeen and Walter H. Brattein, Bell Telephone Laboratories, which received the Nobel Prize in Physics in 1956. Probably, everybody thinks that it was recognized

immediately as a major invention.
Chip Design and Implementation from a Practical Viewpoint Focusing on chip implementation, Low-Power NoC for High-Performance SoC Design provides practical knowledge and real examples of how to use network on chip (NoC) in the design of system on chip (SoC). It discusses many architectural and theoretical studies on NoCs, including design methodology, topology exploration, quality-of-service guarantee, low-power design, and implementation trials. The Steps to Implement NoC The book covers the full spectrum of the subject, from theory to actual chip design using NoC. Employing the Unified Modeling Language (UML) throughout, it presents complicated concepts, such as models of computation and communication–computation partitioning, in a manner accessible to laypeople. The authors provide guidelines on how to simplify complex networking theory to design a working chip. In addition, they explore the novel NoC techniques and implementations of the Basic On-Chip Network (BONE) project. Examples of real-time decisions, circuit-level design, systems, and chips give the material a real-world context. Low-Power NoC and Its Application to SoC Design Emphasizing the application of NoC to SoC design, this book shows how to build the complicated interconnections on SoC while keeping a low power consumption.

Robotics and control are both research and application domains that have been frequently engineered through the use of interdisciplinary approaches like cybernetics. Cognition is a particular concept of this approach, abstracted from the context of living organisms to that of artificial devices, and is concerned with knowledge acquisition and understanding through thought, experience, and the senses. Cognitive robotics and control refer to knowledge processing as much as knowledge generation from problem understanding, leading to special forms of architectures that enable systems to behave in an autonomous way. The main aim of this book is to highlight emerging applications and address recent breakthroughs in the domain of cognitive robotics and control and related areas. Procedures, algorithms, architectures, and implementations for reasoning, problem solving, or decision making are considered in the domain of robotics and control.

This book constitutes the refereed proceedings of the 22nd International Conference on Information and Communications Security, ICICS 2020, held in Copenhagen, Denmark*, in August 2020. The 33 revised full papers were carefully selected from 139 submissions. The papers focus in topics about computer and communication security, and are organized in topics of security and cryptography. *The conference was held virtually due to the

COVID-19 pandemic.

In the research area of computer science, practitioners are constantly searching for faster platforms with pertinent results. With analytics that span environmental development to computer hardware emulation, problem-solving algorithms are in high demand. Field-Programmable Gate Array (FPGA) is a promising computing platform that can be significantly faster for some applications and can be applied to a variety of fields. FPGA Algorithms and Applications for the Internet of Things provides emerging research exploring the theoretical and practical aspects of computable algorithms and applications within robotics and electronics development. Featuring coverage on a broad range of topics such as neuroscience, bioinformatics, and artificial intelligence, this book is ideally designed for computer science specialists, researchers, professors, and students seeking current research on cognitive analytics and advanced computing.

This book presents a selection of papers representing current research on using field programmable gate arrays (FPGAs) for realising image processing algorithms. These papers are reprints of papers selected for a Special Issue of the Journal of Imaging on image processing using FPGAs. A diverse range of topics is covered, including parallel soft processors, memory management, image filters, segmentation, clustering,

image analysis, and image compression. Applications include traffic sign recognition for autonomous driving, cell detection for histopathology, and video compression. Collectively, they represent the current state-of-the-art on image processing using FPGAs.

This book is devoted to embedded systems (ESs), which can now be found in practically all fields of human activity. Embedded systems are essentially a special class of computing systems designed for monitoring and controlling objects of the physical world. The book begins by discussing the distinctive features of ESs, above all their cybernetic-physical character, and how they can be designed to deliver the required performance with a minimum amount of hardware. In turn, it presents a range of design methodologies. Considerable attention is paid to the hardware implementation of computational algorithms. It is shown that different parts of complex ESs could be implemented using models of finite state machines (FSMs). Also, field-programmable gate arrays (FPGAs) are very often used to implement different hardware accelerators in ESs. The book pays considerable attention to design methods for FPGA-based FSMs, before the closing section turns to programmable logic controllers widely used in industry. This book will be interesting and useful for students and postgraduates in the area of Computer Science, as well as for designers

of embedded systems. In addition, it offers a good point of departure for creating embedded systems for various spheres of human activity.

This book constitutes the proceedings of the 31st Australasian Joint Conference on Artificial Intelligence, AI 2018, held in Wellington, New Zealand, in December 2018. The 50 full and 26 short papers presented in this volume were carefully reviewed and selected from 125 submissions. The paper were organized in topical sections named: agents, games and robotics; AI applications and innovations; computer vision; constraints and search; evolutionary computation; knowledge representation and reasoning; machine learning and data mining; planning and scheduling; and text mining and NLP.

This comprehensive textbook on the field programmable gate array (FPGA) covers its history, fundamental knowledge, architectures, device technologies, computer-aided design technologies, design tools, examples of application, and future trends. Programmable logic devices represented by FPGAs have been rapidly developed in recent years and have become key electronic devices used in most IT products. This book provides both complete introductions suitable for students and beginners, and high-level techniques useful for engineers and researchers in this field. Differently developed from usual integrated circuits, the FPGA has unique

structures, design methodologies, and application techniques. Allowing programming by users, the device can dramatically reduce the rising cost of development in advanced semiconductor chips. The FPGA is now driving the most advanced semiconductor processes and is an all-in-one platform combining memory, CPUs, and various peripheral interfaces. This book introduces the FPGA from various aspects for readers of different levels. Novice learners can acquire a fundamental knowledge of the FPGA, including its history, from Chapter 1; the first half of Chapter 2; and Chapter 4. Professionals who are already familiar with the device will gain a deeper understanding of the structures and design methodologies from Chapters 3 and 5. Chapters 6–8 also provide advanced techniques and cutting-edge applications and trends useful for professionals. Although the first parts are mainly suitable for students, the advanced sections of the book will be valuable for professionals in acquiring an in-depth understanding of the FPGA to maximize the performance of the device.

This book constitutes the thoroughly refereed conference proceedings of the 12th International Conference on Cognitive Radio Oriented Wireless Networks, CROWNCOM 2017, held in Lisbon, Portugal, in September 2017. The 28 revised full papers presented were carefully reviewed and selected from numerous submissions and cover the

evolution of cognitive radio technology pertaining to 5G networks. The papers are clustered to topics on spectrum management; network management; trials, test beds, and tools; PHY and sensing; spectrum management.

This book constitutes the proceedings of the 14th International Workshop on Open MP, IWOMP 2018, held in Barcelona, Spain, in September 2018. The 16 full papers presented in this volume were carefully reviewed and selected for inclusion in this book. The papers are organized in topical sections named: best paper; loops and OpenMP; OpenMP in heterogeneous systems; OpenMP improvements and innovations; OpenMP user experiences: applications and tools; and tasking evaluations.

Field-Programmable Gate Array (FPGA) technologies have increased in popularity in recent years due to their adaptability and high computing potential. Further research in this area illustrates the potential for further advancements and applications of this useful technology. Field-Programmable Gate Array (FPGA) Technologies for High Performance Instrumentation presents experimental and theoretical research on FPGA-based design and the development of virtual scientific instrumentation that can be used by a broad segment of scientists across a variety of research fields. Focusing on crucial innovations and algorithms for signal processing, data acquisition mechanisms, FPGA-based

hardware design, and parallel computing, this publication is a critical resource for researchers, development engineers, and graduate-level students.

Field Programmable Gate Arrays (FPGAs) are currently recognized as the most suitable platform for the implementation of complex digital systems targeting an increasing number of industrial electronics applications. They cover a huge variety of application areas, such as: aerospace, food industry, art, industrial automation, automotive, biomedicine, process control, military, logistics, power electronics, chemistry, sensor networks, robotics, ultrasound, security, and artificial vision. This book first presents the basic architectures of the devices to familiarize the reader with the fundamentals of FPGAs before identifying and discussing new resources that extend the ability of the devices to solve problems in new application domains. Design methodologies are discussed and application examples are included for some of these domains, e.g., mechatronics, robotics, and power systems.

This book constitutes the refereed proceedings of the 12th International Conference on Computer Vision Systems, ICVS 2019, held in Thessaloniki, Greece, in September 2019. The 72 papers presented were carefully reviewed and selected from 114 submissions. The papers are organized in the

following topical sections; hardware accelerated and real time vision systems; robotic vision; vision systems applications; high-level and learning vision systems; cognitive vision systems; movement analytics and gesture recognition for human-machine collaboration in industry; cognitive and computer vision assisted systems for energy awareness and behavior analysis; and vision-enabled UAV and counter UAV technologies for surveillance and security of critical infrastructures. This book reports on new theories and applications in the field of intelligent systems and computing. It covers computational and artificial intelligence methods, as well as advances in computer vision, current issues in big data and cloud computing, computation linguistics, and cyber-physical systems. It also reports on data mining and knowledge extraction technologies, as well as central issues in intelligent information management. Written by active researchers, the respective chapters are based on papers presented at the International Conference on Computer Science and Information Technologies (CSIT 2017), held on September 5–8, 2017, in Lviv, Ukraine; and at two workshops accompanying the conference: one on inductive modeling, jointly organized by the Lviv Polytechnic National University and the National Academy of Science of Ukraine; and another on project management, which was jointly organized by the

Lviv Polytechnic National University, the International Project Management Association, the Ukrainian Project Management Association, the Kazakhstan Project Management Association, and Nazarbayev University. Given its breadth of coverage, the book provides academics and professionals with extensive information and a timely snapshot of the field of intelligent systems, and is sure to foster new discussions and collaborations among different groups.

Machine learning is a potential solution to resolve bottleneck issues in VLSI via optimizing tasks in the design process. This book aims to provide the latest machine-learning–based methods, algorithms, architectures, and frameworks designed for VLSI design. The focus is on digital, analog, and mixed-signal design techniques, device modeling, physical design, hardware implementation, testability, reconfigurable design, synthesis and verification, and related areas. Chapters include case studies as well as novel research ideas in the given field. Overall, the book provides practical implementations of VLSI design, IC design, and hardware realization using machine learning techniques. Features: Provides the details of state-of-the-art machine learning methods used in VLSI design Discusses hardware implementation and device modeling pertaining to machine learning algorithms Explores machine learning for various VLSI architectures and

reconfigurable computing Illustrates the latest techniques for device size and feature optimization Highlights the latest case studies and reviews of the methods used for hardware implementation This book is aimed at researchers, professionals, and graduate students in VLSI, machine learning, electrical and electronic engineering, computer engineering, and hardware systems.

This book suggests and describes a number of fast parallel circuits for data/vector processing using FPGA-based hardware accelerators. Three primary areas are covered: searching, sorting, and counting in combinational and iterative networks. These include the application of traditional structures that rely on comparators/swappers as well as alternative networks with a variety of core elements such as adders, logical gates, and look-up tables. The iterative technique discussed in the book enables the sequential reuse of relatively large combinational blocks that execute many parallel operations with small propagation delays. For each type of network discussed, the main focus is on the step-by-step development of the architectures proposed from initial concepts to synthesizable hardware description language specifications. Each type of network is taken through several stages, including modeling the desired functionality in software, the retrieval and automatic conversion of key functions, leading to specifications for optimized hardware

modules. The resulting specifications are then synthesized, implemented, and tested in FPGAs using commercial design environments and prototyping boards. The methods proposed can be used in a range of data processing applications, including traditional sorting, the extraction of maximum and minimum subsets from large data sets, communication-time data processing, finding frequently occurring items in a set, and Hamming weight/distance counters/comparators. The book is intended to be a valuable support material for university and industrial engineering courses that involve FPGA-based circuit and system design. Field programmable gate arrays (FPGAs) are an increasingly popular technology for implementing digital signal processing (DSP) systems. By allowing designers to create circuit architectures developed for the specific applications, high levels of performance can be achieved for many DSP applications providing considerable improvements over conventional microprocessor and dedicated DSP processor solutions. The book addresses the key issue in this process specifically, the methods and tools needed for the design, optimization and implementation of DSP systems in programmable FPGA hardware. It presents a review of the leading-edge techniques in this field, analyzing advanced DSP-based design flows for both signal flow graph-(SFG-) based and dataflow-based implementation,

system on chip (SoC) aspects, and future trends and challenges for FPGAs. The automation of the techniques for component architectural synthesis, computational models, and the reduction of energy consumption to help improve FPGA performance, are given in detail. Written from a system level design perspective and with a DSP focus, the authors present many practical application examples of complex DSP implementation, involving: high-performance computing e.g. matrix operations such as matrix multiplication; high-speed filtering including finite impulse response (FIR) filters and wave digital filters (WDFs); adaptive filtering e.g. recursive least squares (RLS) filtering; transforms such as the fast Fourier transform (FFT). FPGA-based Implementation of Signal Processing Systems is an important reference for practising engineers and researchers working on the design and development of DSP systems for radio, telecommunication, information, audio-visual and security applications. Senior level electrical and computer engineering graduates taking courses in signal processing or digital signal processing shall also find this volume of interest.

This book covers basic fundamentals of logic design and advanced RTL design concepts using VHDL. The book is organized to describe both simple and complex RTL design scenarios using VHDL. It gives practical information on the issues in ASIC

prototyping using FPGAs, design challenges and how to overcome practical issues and concerns. It describes how to write an efficient RTL code using VHDL and how to improve the design performance. The design guidelines by using VHDL are also explained with the practical examples in this book. The book also covers the ALTERA and XILINX FPGA architecture and the design flow for the PLDs. The contents of this book will be useful to students, researchers, and professionals working in hardware design and optimization. The book can also be used as a text for graduate and professional development courses.

This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and

Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.

Using the new OpenCL (Open Computing Language) standard, you can write applications that access all available programming resources: CPUs, GPUs, and other processors such as DSPs and the Cell/B.E. processor. Already implemented by Apple, AMD, Intel, IBM, NVIDIA, and other leaders, OpenCL has outstanding potential for PCs, servers, handheld/embedded devices, high performance computing, and even cloud systems. This is the first comprehensive, authoritative, and practical guide to OpenCL 1.1 specifically for working developers and software architects. Written by five leading OpenCL authorities, OpenCL Programming Guide covers the entire specification. It reviews key use cases, shows how OpenCL can express a wide range of parallel algorithms, and offers complete reference material on both the API and OpenCL C programming language. Through complete case studies and downloadable code examples, the authors show how to write complex parallel programs that decompose workloads across many different devices. They also present all the essentials of OpenCL software performance optimization, including probing and adapting to hardware. Coverage includes Understanding OpenCL's architecture, concepts,

terminology, goals, and rationale Programming with OpenCL C and the runtime API Using buffers, sub-buffers, images, samplers, and events Sharing and synchronizing data with OpenGL and Microsoft's Direct3D Simplifying development with the C++ Wrapper API Using OpenCL Embedded Profiles to support devices ranging from cellphones to supercomputer nodes Case studies dealing with physics simulation; image and signal processing, such as image histograms, edge detection filters, Fast Fourier Transforms, and optical flow; math libraries, such as matrix multiplication and high-performance sparse matrix multiplication; and more Source code for this book is available at https://code.google.com/p/opencl-book-samples/ Engineering the Complex SOC The first unified hardware/software guide to processor-centric SOC design Processor-centric approaches enable SOC designers to complete far larger projects in far less time. Engineering the Complex SOCis a comprehensive, example-driven guide to creating designs with configurable, extensible processors. Drawing upon Tensilica's Xtensa architecture and TIE language, Dr. Chris Rowen systematically illuminates the issues, opportunities, and challenges of processor-centric design. Rowen introduces a radically new design methodology, then covers its essential techniques: processor configuration, extension, hardware/software co-generation, multiple

processor partitioning/communication, and more. Coverage includes: Why extensible processors are necessary: shortcomings of current design methods Comparing extensible processors to traditional processors and hardwired logic Extensible processor architecture and mechanisms of processor extensibility Latency, throughput, coordination of parallel functions, hardware interconnect options, management of design complexity, and other issues Multiple-processor SOC architecture for embedded systems Task design from the viewpoints of software andhardware developers Advanced techniques: implementing complex state machines, task-to-task synchronization, power optimization, and more Toward a “sea of processors”: Long-term trends in SOC design and semiconductor technology For all architects, hardware engineers, software designers, and SOC program managers involved with complex SOC design; and for all managers investing in SOC designs, platforms, processors, or expertise. PRENTICE HALL Professional Technical Reference Upper Saddle River, NJ 07458 www.phptr.com